(12) UK Patent Application (19) GB (11) 2 365 215 (13) A

(43) Date of A Publication 13.02.2002

(21) Application No 0101254.1

(22) Date of Filing 18.01.2001

(30) Priority Data
(31) 09533851 (32) 23.03.2000 (33) US

(71) Applicant(s)
International Business Machines Corporation
(Incorporated in USA - New York)
Armonk, New York 10504, United States of America

(72) Inventor(s)
Vincent James McGahay
Ernest Levine

(74) Agent and/or Address for Service
IBM United Kingdom Limited
Intellectual Property Department, Hursley Park,
WINCHESTER, Hampshire, SO21 2JN,
United Kingdom

(51) INT CL[7]
H01L 21/768 21/02 23/532

(52) UK CL (Edition T)
H1K KHAAB K4C11 K4C2B K4C23

(56) Documents Cited
EP 0472804 A2 WO 98/32175 A1
US 6015749 A US 5913147 A

(58) Field of Search
UK CL (Edition S) H1K KHAAB KHAAX KHAC KHAX KJAA KJAB KJACX KJAD .
INT CL[7] H01L
ONLINE: WPI, EPODOC, JAPIO, INSPEC

(54) Abstract Title

Composite diffusion barrier for protecting copper interconnects in low dielectric constant materials from oxidation

(57) A composite diffusion barrier (26,28) protects copper structure (30) from oxidation in the presence of oxygen or water in an integrated circuit. The copper structure (30) may be a dual damascene conductor with conductor (32) and via portions (34). The composite barrier includes dense diffusion barrier (28), which may be made of tantalum and/or tantalum nitride, and barrier film (26) capable of forming a protective oxide in a self limiting manner in the presence of oxygen or water. Oxidation of barrier film (26) enables in-situ repair of defects such as pinholes in the diffusion barrier (28). The barrier film (26) may contain aluminium, silicon or Cu_3Ge. The composite barrier (26,28) is situated in a semiconductor device, which includes an insulator layer (20), which may have low dielectric constant k and high permeability. The device may also have nitride cap (38).

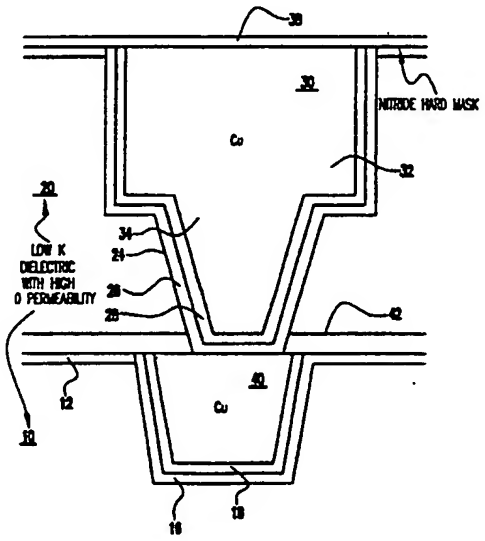

FIG.1

GB 2 365 215 A

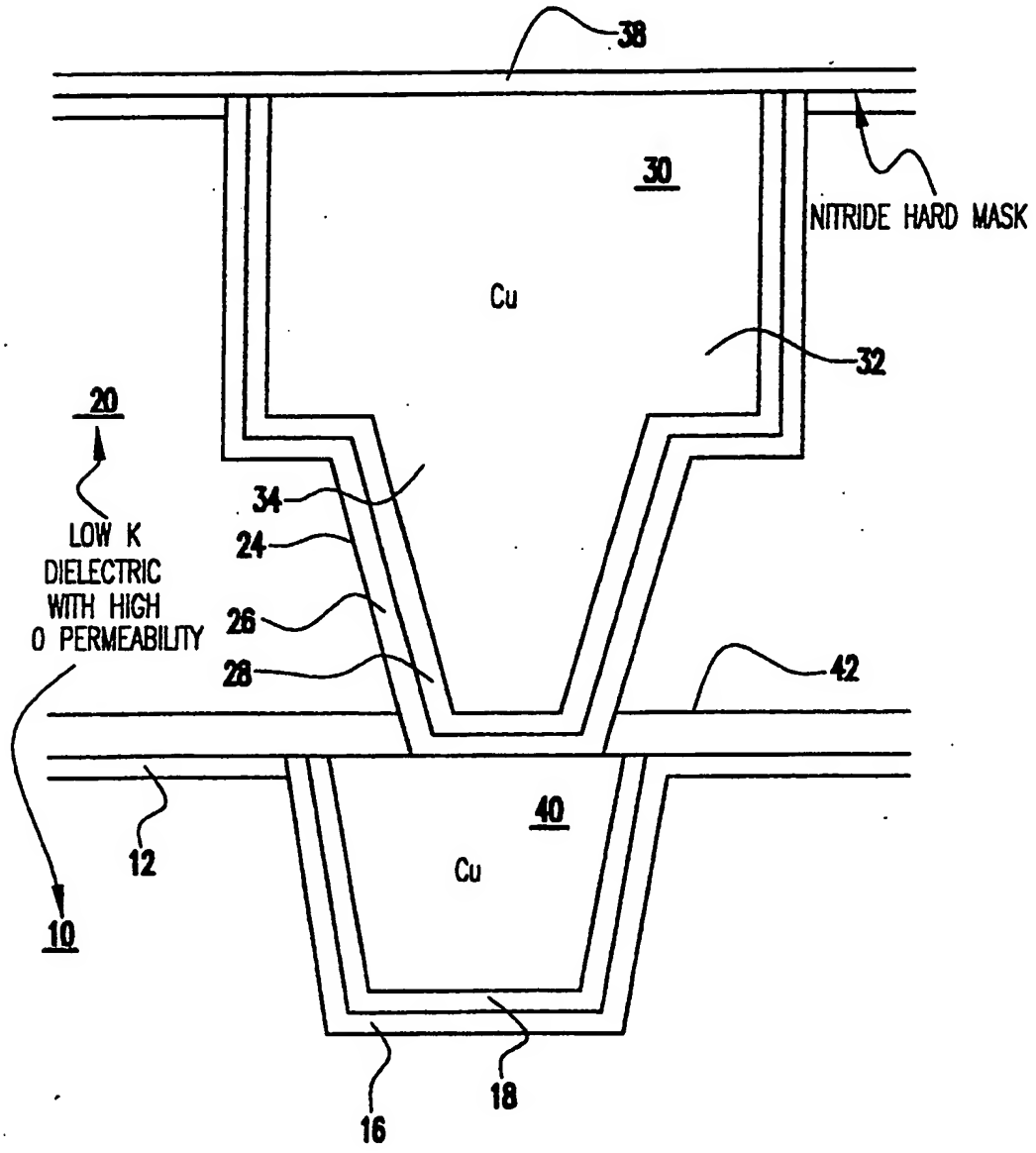
38
30
NITRIDE HARD MASK
Cu
32
20
LOW K
DIELECTRIC
WITH HIGH
0 PERMEABILITY
34
24
26
28
42
40
Cu
12
10
16
18

FIG.1

STRUCTURE FOR PROTECTING COPPER INTERCONNECTS IN LOW DIELECTRIC CONSTANT MATERIALS FROM OXIDATION

The present invention generally relates to integrated circuit devices and, more particularly, to integrated circuit devices using both copper interconnects and low dielectric coefficient ("low K") insulators.

Recognized benefits in performance, functionality and manufacturing economy have provided strong incentives for increasing the integration density of integrated circuit devices. While increased manufacturing economy and functionality derives from the increased number of devices which can be formed in the course of a given group of material treatment processes (e.g. lithography, etching, deposition, implantation and the like), increased performance derives from reduced signal propagation time (and, generally, noise immunity) when switching elements are placed in greater physical proximity. Shorter interconnection lengths generally reduce both resistance and capacitance of the connection and produce faster rise and fall times of signal transitions while reduced capacitance generally results in reduced capacitively coupled noise between conductors.

However, increased signal transition speed can also increase the magnitude of noise that may be capacitively coupled between conductors while increased proximity of interconnects tends to increase capacitance between them. Therefore, at the present state of the art, dielectrics exhibiting a low dielectric constant (e.g. K = 3.0 or lower) are being investigated to minimize capacitance between conductors having given dimensions and spacing. At the same time, copper has been found to provide distinct performance advantages in comparison with less highly conductive materials for interconnects while providing distinct advantages in economy in comparison with some other materials such as silver and gold and without introducing process complexities as are presented by some refractory metals. Copper is also less subject to metal migration than some other metals, notably aluminum.

However, copper is subject to oxidation in the presence of oxygen or water even when enclosed within a semiconductor structure since oxygen is often available within the semiconductor structure, itself, since current dielectric materials often include or are principally formed of oxides. Alternatively, oxygen or water may be diffused therethrough although oxygen is generally tightly bound in such oxides and diffusion of water molecules is generally very limited. Therefore, the likelihood of failure due to oxidation of copper in integrated circuits of conventional construction is relatively

low over the projected lifetime of a conventional chip. Nevertheless, at currently possible and foreseeable integration densities, it is anticipated that such oxidation may be substantially more critical since the widths and thicknesses of copper interconnects will be of reduced size.

Therefore, it is known to form fine, low resistance, interconnects in layered structures, generally including an adhesion layer (e.g. tantalum or tantalum nitride), a copper layer, and a sealing/protection layer of, for example, silicon nitride. However, such a sealing/protection layer is expensive if formed of gold and the process complexity in forming multi-layer conductors is significant. Other dense barrier material films are known and can be employed but assurance that such a film will be defect free is difficult since sufficiently dense materials such as tantalum and tantalum nitride have a tendency to form pinhole defects sufficient to allow oxygen or water diffusion.

Further, it can be appreciated that the inclusion of diffusion barriers consumes finite space and may impose a limitation on integration density if formed with a transverse dimension of the minimum feature size. In this regard, it can be further appreciated that diffusion can often occur most easily from the edge of a chip which has been diced from a wafer and in which all interfaces between layers are exposed unless edge seals are provided and which involve substantial manufacturing difficulty. Even if barriers are formed in a self-aligned manner to obtain smaller dimensions, the barrier may serve to reduce a critical dimension of another structure such as a copper conductor.

If oxidation of copper occurs to even a slight degree, it can also be appreciated that resistance and signal propagation time will be increased. This effect may occur over an extended period of time after apparatus including the integrated circuit is placed in service. Given that it is principally very high-performance integrated circuit designs which will include copper interconnects, the probability of a criticality being reached is substantial while failure or error due to increase of propagation time will be highly unpredictable.

It is therefore an object of the present invention to provide a highly effective barrier layer for preventing diffusion of water and/or oxygen which can be reliably formed with reduced cost and process complexity consistent with high integration density and which can protect copper from oxidation damage in particularly minute structures.

It is another object of the invention to provide a more easily and reliably manufactured diffusion barrier in an integrated circuit device which include copper structures and which will effectively prevent oxidation of copper structures therein and compromise or deterioration of performance.

It is a further object of the invention to provide a technique and structure for prevention of oxidation of copper structures which are used in integrated circuits in combination with other materials which may provide otherwise unobtainable electrical characteristics but which may tend to enhance diffusion of oxygen and/or water within the integrated circuit.

It is yet another object of the invention to provide a technique of improving robustness and integrity of dense diffusion barrier layers in semiconductor devices.

In order to accomplish these and other objects of the invention, a semiconductor device is provided including an insulating layer, a copper structure, and a composite diffusion barrier between the insulating layer and said copper structure comprising a layer of dense material, and a film of material capable of forming a protective oxide in a self-limiting manner in the presence of oxygen or water.

Preferably the semiconductor device further comprises a protective cap on a surface of said copper structure, and more preferably the protective cap is formed of a nitride. Aptly the copper structure is a damascene conductor, and more aptly copper structure is a double damascene conductor.

The semiconductor device may also suitably include a plurality of insulator layers, at least two of said plurality of insulator layers including a said copper structure and a said composite layer. The insulator used in the device preferably has a dielectric constant of 3.0 or lower.

In a particularly preferred embodiment the film of material includes at least one material from the group consisting of aluminium, silicon and Cu_3Ge.

In accordance with another aspect of the invention, a method of making a semiconductor device is provided, including a step of forming a composite conductor including a body of copper, a diffusion barrier layer of dense material, and a layer of material capable of forming a protective oxide in a self-limiting manner in the presence of oxygen or water, and a further step of forming an insulator wherein said layer of material capable of forming a

protective oxide is interposed between the insulator and said body of copper and the diffusion barrier.

Preferably in the method of making the semiconductor device the composite conductor is formed in a recess in said insulator, and more preferably the method includes the further step of forming a protective cap on a surface of said body of copper.

Aptly the method includes the further steps of forming a further insulator over said insulator and said composite conductor, and forming a further composite conductor in said further insulating layer.

In a particularly performed embodiment the material capable of forming a protective oxide includes at least one material form the group consisting of aluminium, silicon and Cu_3Ge.

In accordance with a further aspect of the invention, a method of in-situ repair of a diffusion barrier in a semiconductor device is provided, comprising the step of oxidizing a material capable of forming a protective oxide in the presence of oxygen or water in a self-limiting manner and in contact with the diffusion barrier.

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a cross-sectional view of a layered semiconductor structure taken at a conductor connection therein in accordance with an exemplary preferred embodiment of the invention.

Referring now to the drawings, and more particularly to Figure 1, there is shown a cross-sectional view of a portion of an integrated circuit including an exemplary embodiment of the invention. Since the preferred application of the invention is for providing protection against oxidation for copper conductors and interconnects including lines and vias, only conductors in different layers with a connecting via are shown and will be found sufficient to the understanding and practice of the invention by those skilled in the art. It should also be understood that the conductors shown are formed in accordance with a preferred Damascene process but the layering of materials can be applied (in the reverse order) to conductors formed on the surface of

layers and covered with a passivation layer as well as Damascene conductors formed within trenches and/or vias.

Further, the inventors have discovered that low dielectric coefficient ("low K", K = 3.0 or lower) materials such as organic polymers and porous insulators are often poor barriers against diffusion of oxygen and/or water compared to dielectrics such as silicon oxide, silicon nitride, silicon germanium nitride and the like. A chip diced from a wafer having copper interconnects within it is highly susceptible to copper oxidation, particularly if low K materials are also used therein. This susceptibility to oxidation exists even if a dense metal barrier such as tantalum and/or tantalum nitride is also provided since it is difficult to assure that such barriers will be defect free and devoid of "pinholes" which can allow diffusion of oxygen and/or water therethrough. While materials suitable for a dense barrier will form oxides or other compounds, it does not appear that such oxides or other compounds have properties such that any pinhole or other defects which could occur would be effectively plugged.

Accordingly, the invention provides for an additional barrier layer between copper structures (or, preferably, a dense barrier layer covering the copper structures) and an insulator such as a low K material. This additional barrier layer is of a material which is known to grow a self-limiting protective oxide which provides an in-situ oxidation barrier. Preferably (e.g. for a Damascene conductor), this additional barrier layer is formed as an underlayer to a dense barrier layer on which the copper structure is deposited, as will now be described in detail. The self-limiting protective oxide thus forms wherever oxygen or water can diffuse in the vicinity of a copper structure and not only protects the remainder of the underlayer as well as the copper structure it surrounds but also serves to plug any pinhole defects which may be developed in the dense material barrier layer ordinarily provided.

Referring now to Figure 1, an example of a structure employing the invention and a method of manufacture thereof will now be described. It should be appreciated that the structure shown in Figure 1 includes two insulator layers 10 and 20, each having a Damascene conductor formed therein. While the Damascene process, in general, is well-known, for the formation of high quality and structurally robust connectors by depositing metal in a recess in an insulator and planarizing the metal to the surface of the insulator. Figure 1 also includes the barrier film in accordance with the

invention. Therefore, no portion of Figure 1 is admitted to be prior art in regard to the present invention.

The conductor structure 30 in layer 20 is of the so-called double Damascene configuration having a conductor portion 32 and a via portion 34. The Damascene conductor 40 in layer 10, as depicted, corresponds to the more common Damascene conductor configuration but could also represent a portion of a double Damascene structure with a via in front of and/or behind the plane of the page. A double Damascene conductor may be formed in a number of ways familiar to those skilled in the art including a sequence of masking and etching processes on a single insulator layer and sequentially applied and patterned insulator layers and one or more metal deposition and planarization steps to fill the shaped recess. The particular process which would be preferred is generally dependent on the particular materials used, particularly the properties of the insulator and the processes which can be reliably performed upon it.

The particular method employed in the generalized Damascene or double Damascene process as known and practiced in the art is not important to the successful practice of the invention. Similarly, the invention is not limited to structures formed in a recess in an insulator but is also applicable to surface structures covered by an insulator. In the latter case, the reverse of the sequence (with modification of the patterning processes as will be evident to those skilled in the art) which will now be described would be suitable for successful practice of the invention in regard to such surface structures. Therefore, while the following discussion is directed to the preferred embodiment and application of the invention, it will enable the successful practice of the invention, generally, by those skilled in the art.

Starting with insulator layer 10, which can be of a low K material by virtue of the invention, a nitride or other hard and selectively etchable (for use as an etch and/or polish stop) insulator layer 12 is applied on a surface thereof and patterned to form a hard mask. Using the hard mask 12, recesses 14 are formed in insulator layer 10 by any etching process and etchant suitable for the insulator material. Then, in accordance with the invention, a film of metal (e.g. aluminum) or other material (e.g. silicon, germanium , Cu3Ge) known to form a self-limiting protective oxide is applied to the interior of the recess to form layer 16, preferably by sputtering, evaporation or chemical vapor deposition (CVD). A very thin barrier film of about 100 Angstroms or less will generally suffice as long as the thickness is sufficient to provide complete coverage of the interior of recess 14.

Then a diffusion barrier layer 18 of dense material (e.g. tantalum and/or tantalum nitride) is applied to form layer 18 in any known manner. It should be recalled that inclusion of this barrier layer (18) of dense material is known for protection against diffusion of oxygen and/or water but subject to defects such as pinholes which allow some diffusion to occur.

The remainder of the recess is then filled with copper to form a high conductivity connection or other structure 40 and a nitride cap 42 is applied. The nitride cap is then patterned to the copper at desired locations of electrical connections (e.g. a via) thereto. The next insulator layer 20 may then be applied and patterned, possibly as a sequence of patterned layers, if necessitated by the materials as alluded to above and the process described above repeated to form a barrier film 26 of material capable of forming a protective oxide in a self-limiting manner and a diffusion barrier layer 28 of dense material lining recess 24 and copper via 34 and conductor 32, followed by nitride cap 38. This process may be repeated as desired to form additional conductors in additional insulator layers.

In the completed structure of Figure 1 it can be appreciated that the interior of the recess in which the copper structure is formed is lined with a diffusion barrier of dense material and a barrier film of material which forms a protective oxide. When oxygen or water capable of oxidizing copper is diffused through the insulator 10, 20 reaches the barrier film 16, 28 a protective oxide is formed in a self-limiting manner which not only protects the remainder of the film but serves to plug any defects in the dense material barrier layer 18, 28 which may be present. This self-limiting oxidation thus protects and effectively repairs defects in the dense material, in-situ through any of several processes and resulting effects or a combination thereof, whereas oxidation of copper is not self-limiting,

The nitride cap covering the copper structure is generally a sufficient diffusion barrier and, when limited to such a small area and volume relative to the thickness of a low K insulator layer, does not significantly increase the net dielectric coefficient significantly. In any event, capacitance between conductors 32 and 40 in the vicinity of an ohmic connection therebetween is substantially unimportant to the coupling of noise of signal propagation time.

In contrast, all material within the recesses is substantially conductive and capacitance to other conductive structures is minimized by use of only the low K material. Note that the barrier film 26 and diffusion

barrier 28 can extend across the bottom of a via and an electrical connection made therethrough. The formation of the barrier film 26 against the nitride cap 42 is a sufficient barrier to prevent oxidation within the barrier film 26 with the via connection to copper structure 40. Any protective oxidation occurring at or in the barrier films is of insufficient relative volume or area to significantly increase net dielectric constant and capacitance.

In view of the foregoing, it is seen that the invention provides a technique for improving the quality and robustness of a diffusion barrier of dense material and the repair of defects which tend to form therein. The invention thus substantially prevents deterioration of copper structures through oxidation even when low K materials which favor diffusion of oxygen and/or water are employed as insulators. Other expensive and marginally effective measures such as sealing edges of a chip are rendered unnecessary and obsolete by the invention. The invention can be inexpensively and reliably applied to any copper structure in an integrated circuit and serves to preserve and allow maximization of signal propagation speed and noise immunity.

While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

1. A semiconductor device including
an insulating layer,
a copper structure, and
a composite diffusion barrier between said insulating layer and said copper structure comprising
a layer of dense material, and
a film of material capable of forming a protective oxide in a self-limiting manner in the presence of oxygen or water.

2. A device as recited in claim 1, further comprising a protective cap on a surface of said copper structure.

3. A device as recited in claim 2, wherein said protective cap is formed of a nitride,

4. A device as recited in claim 1, wherein said copper structure is a damascene conductor.

5. A device as recited in claim 1, wherein said copper structure is a double damascene conductor.

6. A device as recited in claim 1, including a plurality of insulator layers, at least two of said plurality of insulator layers including a said copper structure and a said composite layer.

7. A device as recited in claim 1, wherein said insulator has a dielectric constant of 3.0 or lower.

8. A device as recited in claim 1, wherein said film of material includes at least one material from the group consisting of aluminum, silicon and Cu3Ge.

9. A method of making a semiconductor device, including a step of
forming a composite conductor including
a body of copper
a diffusion barrier layer of dense material, and
a layer of material capable of forming a protective oxide in a self-limiting manner in the presence of oxygen or water, and a further step of

forming an insulator wherein said layer of material capable of forming a protective oxide is interposed between said insulator and said body of copper and said diffusion barrier.

10. A method as recited in claim 9, wherein said composite conductor is formed in a recess in said insulator.

11. A method as recited in claim 9, including the further step of forming a protective cap on a surface of said body of copper.

12. A method as recited in claim 9, including the further steps of

forming a further insulator over said insulator and said composite conductor, and

forming a further composite conductor in said further insulating layer.

13. A method as recited in claim 9, wherein said material capable of forming a protective oxide includes at least one material from the croup consisting of aluminum, silicon and Cu3Ge.

14. A method of in-situ repair of a diffusion barrier in a semiconductor device, comprising the step of

oxidizing a material capable of forming a protective oxide in the presence of oxygen or water in a self-limiting manner, said material being in contact with said diffusion barrier.

INVESTOR IN PEOPLE

Application No:	GB 0101254.1	**Examiner:**	T P Marlow
Claims searched:	1 to 14	**Date of search:**	15 November 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1K: (KHAAB) (KHAAX) (KHAC) (KHAX) (KJAA) (KJAB) (KJAD) (KJACX)

Int Cl (Ed.7): H01L

Other: ONLINE: WPI, EPODOC, JAPIO, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0472804 A2	IBM - see insulator layer (16), copper structure (14) and barrier containing dense material of tungsten (12) and silicon film (10) in Fig. 1	1,7-10, 13,14
X	WO 98/32175	PHILIPS - see aluminium layer (7) on SiO_2 layer (7) and composite diffusion barrier having diffusion barrier layer (11) and aluminium layer (13) in Fig. 1	1-14
X	US 6015749	TAIWAN SEMICONDUCTOR - see Fig. 10 showing insulating layer (2), copper structure (7), composite diffusion barrier having TiN layer (4) and Cu_3Ge barrier (56)	1-14
X	US 5913147	ADVANCED MICRO DEVICES - see diffusion barrier layer (22) and copper/aluminium alloy film (24) and copper/aluminium structure (54) in Figs. 2 to 5	1-14

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.